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(54) Semiconductor structure with abrupt doping profile

(57) A structure and method of forming an abrupt doping profile are described. A perferred embodiment incorporates a substrate 32, a first epitaxial layer 36 of Ge less than the critical thickness and having a P or As concentration greater than $5x10^{19}$ atoms/cc, and a second epitaxial layer 40 having a change in concentration in its first 40Å from the first layer of greater than $1x10^{19}$ P atoms/cc. In another preferred embodiment, a layer of SiGe having a Ge content greater than 0.5 may be selectively amorphized and recrystalized with respect to other layers in a layered structure. The invention addresses the problem of forming abrupt phosphorus profiles in Si and SiGe layers or films in semiconductor structures such as CMOS, MODFET's, and HBT's.

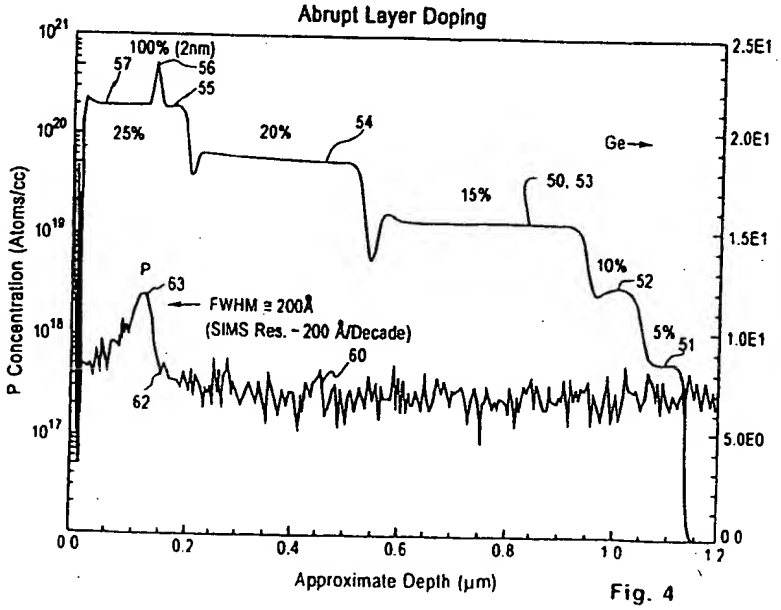

Fig. 4

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Description

This invention relates to semiconductor films with steep doping profiles.

In-situ phosphorus doping in epitaxial Si and SiGe films or layers using PH_3 has been known to demonstrate a very slow incorporation rate of P due to the "poisoning effect" of phosphine on the Si(100) surface. An example of such a doping behavior is shown in Figure 1 by curve 11. Curve portion 13-14 of curve 11 shows the slow "transient" trailing edge observed in the SIMS profile and corresponds to the slow incorporation rate of P into the silicon film. In Fig. 1 the ordinate represents P concentration in atoms/cc and the abscissa represents depth in angstroms.

The incorporation of P into a Si layer is increased by the addition of a Ge containing gas (7%) along with phosphine in the reaction zone of a UHV-CVD reactor and has been described in US Patent 5,316,958 which issued May 31, 1994. The phosphorus dopant was incorporated during UHV-CVD in the proper substitutional sites in the silicon lattice as fully electrically active dopants. The amounts of Ge used were small enough that the primary band gap reduction mechanism is the presence of the n-type dopants at relatively high levels instead of the effect of the Ge In '958. Fig. 2 shows phosphorus being incorporated into a Si layer during UHV-CVD with and without the addition of 7% Ge containing gas. With 7% Ge containing gas, a decade increase in P concentration would be incorporated in 250 to 500Å (25-50nm) into a silicon layer as shown, for example, by the rate of incorporation from 7×10^{18} atoms/cc to 5×10^{19} atoms/cc in Fig. 2 of '958.

Another well known problem associated with in-situ phosphorus or boron doping in silicon CVD is its "memory effect" as shown by curve portion 15-16 in Fig. 1 for the case of phosphorus herein which tends to create an undesirable high level of dopant in the background due to its "autodoping behavior". This "memory effect" is also evident in the SIMS analysis shown in Fig. 1. The "memory effect" corresponds to a very slow fall or decrease in the phosphorus concentration which stems from a residual background autodoping effect. Hence, in-situ doping typically generates a very undesirable "smearing out" of the dopant profile in silicon films formed by CVD.

Fig. 2 shows curve 11 which is the same as shown Fig. 1 and which illustrates the doping profile of the prior art using PH_3. Curve 20 shows a desired or targeted profile having a width of 100Å (10nm) In Fig 2, the ordinate represents P concentration in atoms/cc and the abscissa represents depth in Angstroms Curve 11 has a dopant profile of at least 5 times wider or thicker than the targeted profile of 100Å (10nm) in width or in depth as shown by curve 20.

As device dimensions shrink and especially for future complementary metal oxide semiconductor (CMOS) logic. MODFET's, and HBT's incorporating SiGe layers. very thin layer structures having a width or thickness of 5-20nm of high doping P concentrations will be needed which are impossible to obtain with present technology at this point using present ultra high vacuum-chemical vapor deposition (UHV-CVD) or standard silicon CVD processing.

Accordingly, the present invention provides a structure having an abrupt doping profile comprising:

a single crystal semiconductor substrate having an upper surface,
a first epitaxial layer of Ge over said upper surface, said first epitaxial layer having a thickness less than the critical thickness, and having a concentration of dopant greater than 5×10^{19} atoms/cc, said dopant being selected from the group consisting of phosphorus and arsenic, and
a second epitaxial layer of a semiconductor material over said first epitaxial layer.

In the preferred embodiment, said second layer comprises a material selected from the group consisting of Si and SiGe, has a concentration change from said first layer into 40Å (4nm) of said second layer of greater than 1×10^{19} atoms/cc, a thickness of at least 300Å (30nm), and a doping of phosporus less than 5×10^{16} atoms/cc for a predetermined thickness after its initial 300Å (30nm) thickness. It is also preferred that said first layer has a thickness in the range from 0.5 to 2 nm, and that the structure further includes a third epitaxial layer of semiconductor material having a doping profile with a dopant concentration less than 5×10^{16} atoms/cc.

The invention further provides a method for forming an abrupt doping profile comprising the steps of:

providing a single crystal semiconductor substrate having a major upper surface,
forming a first epitaxial layer of Ge over said upper surface, said first epitaxial layer having a thickness less than the critical thickness,
said step of forming the first epitaxial layer including the step of incorporating a concentration of dopant greater than 5×10^{19} atoms/cc, said dopant being selected from the group consisting of phosphorus and arsenic, and
forming a second epitaxial layer of a semiconductor material over said first epitaxial layer.

It is preferred that said step of providing comprises providing a plurality of substrates, each substrate having a major upper surface, and wherein said steps of forming said first and second epitaxial layers are performed with respect to said plurality of substrates.

It is also preferred that said step of forming said first epitaxial layer further includes the steps of placing said substrate in a CVD reactor and flowing a germanium containing gas and a dopant containing gas, wherein said step of forming said first epitaxial layer further includes the step of adjusting the growth rate of said first

epitaxial layer as a function of time by changing the flow rate of said germanium containing gas, with said step of forming said first epitaxial layer being terminated prior to reaching the critical thickness of said first epitaxial layer.

Likewise, it is also preferred that said step of forming said second epitaxial layer further includes the steps of placing said substrate in a CVD reactor and flowing a silicon containing gas and a dopant containing gas, said dopant being selected from the group consisting of phosphorus and arsenic, wherein said step of forming said second epitaxial layer further includes the step of adjusting the flow rate of said dopant containing gas as a function of time.

Preferably said step of forming said second epitaxial layer includes after the step of forming said first epitaxial layer, the steps of removing said substrate from said first CVD reactor to a load lock having a controlled atmosphere to prevent oxidation of the surface of said layer, and transferring said substrate to a second CVD reactor having internally exposed surfaces initially free of phosphorus.

It is also preferred that said step of forming said second epitaxial layer includes the steps of:

removing said substrate from said the CVD reactor to a load lock having a controlled atmosphere to prevent oxidation of the surface of said layer,
flowing a silicon containing gas such as $H_2/SiH_4/GeH_4$ into the CVD having heated surfaces to coat said heated surfaces with a third silicon containing layer to cover said heated surfaces that may contain phosphorus containing layers that may have formed during the formation of said first epitaxial layer;
transferring said substrate back into the CVD reactor, and
forming a fourth layer on the upper surface of said second epitaxial layer.

The invention further provides a method for forming abrupt doping within a semiconductor layered structure comprising the steps of:

selectively amorphizing a first layer having a high Ge content greater than 0.5, and
crystallizing said amorphized first layer by solid phase regrowth.

Preferably the step of selectively amorphizing includes the step of ion implantation, and further includes forming second and third layers above said first layer, said second and third layers having a Ge content less than 0.5.

The invention also provides a field effect transistor comprising:

a single crystal substrate having a source region and a drain region with a channel therebetween and a gate electrode above said channel to control charge in said channel, and
a first layer of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic positioned below said channel and extending through said source and drain regions.

In the preferred embodiment, said channel is in a second epitaxial layer selected from the group consisting of Si and SiGe formed over said first layer.

The invention further provides a field effect transistor comprising:

a single crystal substrate,
a first layer of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic formed on said substrate,
a second layer of undoped SiGe epitaxially formed on said first layer,
a third layer of strained undoped semiconductor material selected from the group consisting of Si and SiGe, and
a source region and a drain region with a channel therebetween, and a gate electrode above said channel to control charge in said channel.

The invention further provides a field effect transistor comprising:

a single crystal substrate,
an oxide layer formed on said substrate having an opening,
a gate dielectric and gate electrode formed in said opening over said substrate,
a source and drain region formed in said substrate aligned with respect to said gate electrode,
a dielectric sidewall spacer formed on either side of said gate electrode and above a portion of said source and drain regions,
a first layer of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic selectively positioned over exposed portions of said source and drain regions,
a second layer of semiconductor material selected from the group consisting of Si and SiGe doped with a dopant selected from the group consisting of phosphorus and arsenic epitaxially formed over said first layer to form raised source and drain regions.

In a preferred embodiment, said layer of Ge is in the range from 0.5 to 2 nm thick.

Thus a preferred embodiment of the invention provides a structure having an increasing or decreasing

abrupt doping profile comprising a substrate such as Si or SiGe having an upper surface, a first epitaxial layer of substantially Ge formed over the upper surface, the first layer having a thickness in the range from 0 5 to 2 nm and doped e.g. with phosphorus or arsenic to a level of about $5x10^{19}$ atoms/cc, and a second epitaxial layer of a semiconductor material having any desired concentration of dopants. The second layer may be Si or $Si_{1-x}Ge_x$. The concentration profile from the edge or upper surface of the first layer to 40Å (4nm) into the second layer may change by greater than $1x10^{19}$ dopant atoms/cc.

A preferred method in accordance with the present invention comprises the steps of selecting a substrate having an upper surface, growing a first epitaxial layer of substantially Ge thereover less than its critical thickness and doped with phosphorus to a level of about 5 X 10^{19} atoms/cc, and growing a second epitaxial layer selected from the group consisting of Si and SiGe, the second epitaxial layer having any desired doping profile. The presence of the epitaxial Ge layer accelerates the incorporation rate of the P or As doping into the Ge layer, thereby eliminating the slow transient behavior. The initial, in-situ doping level is determined by the dopant flow in SCCM of the PH_3/He mixture. The final overall doping profile may be controlled as a function of 1/GR where GR is the growth rate of the first and second layer The dopant may be supplied or carried by phosphine (PH_3) or Tertiary Butyl Phosphine (TBP) gas in the case of P and AsH_3 or Tertiary Butyl Arsine (TBA) in the case of As in a UHV-CVD reactor.

To eliminate a background "autodoping effect", a structure with phosphorus doping is preferably transferred to a load chamber or load lock, while the growth chamber is purged of the background phosphorus. This growth/interrupt/growth process involves hydrogen flushing of the UHV-CVD reactor during interrupt Then, a coating of Si or SiGe is grown on the sidewalls and/or heated surfaces of the UHV-CVD reactor at high temperature to isolate, eliminate or cover the residual phosphorus atoms prior to reintroducing the structure for further deposition. Alternatively, a second growth chamber i.e. UHV-CVD reactor coupled to the load chamber may be used where further undoped layers may be deposited with very low levels of phosphorus.

A second epitaxial layer and/or a third epitaxial layer of Si or SiGe may now be grown with a background doping profile that drops or decreases to less than $5x10^{16}$ atoms/cc after a 300Å (30nm) film is grown over the first epitaxial layer of the structure 30

The approach described above is particularly useful for forming abrupt "delta-like" doping in thin layers from 5-20nm thick suitable for Si or SiGe CMOS, modulation-doped field-effect transistors (MODFET's) devices, and heterojunction bipolar transistors (HBT's) using in-situ doping in a ultra high vacuum-chemical vapor deposition (UHV-CVD) reactor

Preferred embodiments of the invention will now be described in detail by way of example only with reference to the following drawings

Fig. 1 is a graph of P concentration versus depth in a SiGe substrate showing an actual concentration profile of the prior art;

Fig. 2 is a graph of P concentration versus depth in a SiGe substrate showing an actual concentration profile compared to a desired profile;

Fig. 3 is a cross section view of a structure according to a first preferred embodiment of the invention;

Fig. 4 is a graph of P dopant concentration versus depth and of Ge in $Si_{1-x}Ge_x$ versus depth;

Fig. 5 is a graph of P concentration versus PH_3/He mixture flow rate in SCCM;

Fig. 6 is a graph of measured conductance versus depth as layers are removed and the projected P concentration versus depth in the layer;

Fig. 7 is a cross section view of a layered structure;

Fig. 8 is a cross section view of a layered structure having an amorphized layer;

Fig. 9 is a cross section view of a structure according to a second preferred embodiment of the invention;

Fig. 10 is a cross section view showing an intermediate step in forming the embodiment of Fig. 11

Fig. 11 is a cross section view showing a FET according to a preferred embodiment of the invention. and

Fig. 12 is a cross section view showing a FET according to another preferred embodiment of the invention.

Referring to the drawings and in particular to Fig. 3, a cross section view of structure 30 having an abrupt phosphorus or arsenic profile or abrupt layer doping (ALD) is shown. A substrate 32 having an upper surface 33 may be for example single crystal Si or SiGe. A first layer 36 of 100% or substantially Ge is epitaxially formed on upper surface 33 having a thickness less than the critical thickness and may be, for example, 0.5 to 2 nm and is doped with P or As.

The effect of the thickness of first layer 36 is not to increase the doping concentration of P or As, but the effect is to increase the sheet dose, which is the doping concentration multiplied by the doped layer thickness The doping concentration is controlled by the flow rate of the dopant source gas and by the growth rate of first layer 36, which in turn, is controlled by the flow rate of the Ge source gas which may be, for example, GeH_4

The critical thickness of a layer is the thickness after which the layer relaxes to relieve strain due to lattice mismatch which for a Ge layer is about 1.04 the lattice spacing of a Si layer. Normally, the mechanism for relieving strain is the generation of crystal lattice defects e.g. misfit dislocations which may propagate to the surface in the form of threading dislocations A relaxed layer is no longer lattice matched to the layer below

First layer 36 is substantially Ge and may be 100% Ge. A second layer 40 comprising Si or SiGe doped to any desired level is formed over first layer 36. Second layer 40 may be formed in a UHV-CVD reactor with a dopant source gas such as PH_3. A Si source gas such as SiH_4 or Si_2H_6 and a Ge source gas such as GeH_4 may be used. A third layer 44 comprising doped or undoped Si or SiGe may be formed in a UHV-CVD reactor over second layer 40.

A UHV-CVD reactor suitable for use in depositing first layer 36, second layer 40 and third layer 44 is available from Leybold-Heraeus Co., Germany and is described in US Patent 5,161,964 which issued Jan. 26, 1993 to B.S. Meyerson and in US Patent 5,607,511 which issued Mar. 4 1997 to B.S. Meyerson which are incorporated herein by reference. The operation of the reactor and suitable methods for depositing Si and SiGe films is described in US patent 5,298,452 which issued Mar. 29, 1994 to B.S. Meyerson and which is incorporated herein by reference.

Referring to Fig. 4, secondary ion mass spectroscopy (SIMS) data was obtained from a multilayered structure of $Si_{1-X}Ge_X$ doped with phosphorus. In Fig. 4, the ordinate on the right side represents Ge relative intensity with respect to curve 50 and the abscissa represents approximate depth in microns below the surface of the multilayered structure. The structure at a depth of 1.17 µm is 100% Si with the amount of Ge, X equal to zero. As shown by level curve portions 51-57 on curve 50, the amount X of Ge is 0.05 at from 1.12 to 1.08 µm, 0.10 at from 1.03 to 0.99 µm, at 0.15 from 0.93 to 0.59 µm, 0.20 from 0.52 to 0.2 µm, 0.25 from 0.2 to 0.17 µm, 1.0 from 0.17 to 0.13 µm, and 0.25 from 0.13 to 0.3 µm, respectively. The layers were epitaxially grown over a single crystal substrate by varying the flow rate of GeH_4. Curve 60 shows the in-situ phosphorus doping in the multilayers as a function of depth using PH_3 as the dopant source gas. In Fig. 4, the ordinate on the left side represents P concentration (atoms/cc) with respect to curve 60 and the abscissa represents depth. The 100% seed layer of 0.5-2nm at the depth of 0.17 µm allows for a very abrupt phoshorus doping profile to occur as shown by curve 60 and particularly at curve portion 62-63, in Fig. 4 and at the same time allows for high doping P concentrations to be achieve controllably as shown by curve 70 in Fig. 5.

Fig. 5 is a graph of the phosphorus concentration (atoms/cc) versus 100 PPM PH_3/He mixture flow (SCCM). In Fig. 5, the ordinate represents phosphorus concentration (atoms/cc) and the abscissa represents flow (SCCM).

Due to the limitation of the SIMS technique to resolve very thin layers, the SIMS result shown in Fig. 4 gives a dopant profile width of about 150-200 Å (15-20nm) at full width half maximum (FWHM). To better resolve the dopant profile, Hall measurements were used to measure and profile the active carriers throughout the doped sample by stepwise etching through the entire doped structure coupled with direct Hall measurement after each etching step.

Fig. 6 is a graph showing the conductance versus depth and showing the phosphorus concentration versus depth in a multilayered structure using direct Hall measurements. In Fig. 6 the ordinate on the left side represents conductance (mS) and the abscissa represents depth below the surface of a multilayered $Si_{1-X}Ge_X$ structure having a layer of 1-2 nm Ge at a depth of 115 nm. Curve 80 shows the conductance as measured versus depth. The conductance increases from 0 at 120 nm to 0.21 at 110 nm. The dopant profile as measured by the electrical measurement is shown by curve 88. Curve 80 and/or its data points were used to generate curve 88 shown in Fig. 6 which shows the actual phosphorus doping profile. Curve 88 was generated by dividing the carrier density as determined from the conductance shown by curve 80 at the respective etched depth by the etch layer thickness. In Fig. 6, the ordinate on the right side represents P concentration (atoms/cc). Curve 86 shows the projected concentration based on curve 88 which shows the peak concentration rising abruptly from less than 1×10^{15} at 121 nm to 5×10^{19} at 115 nm corresponding to a 13Å (1.3nm) per decade rise in P concentration. The FWHM based on curve 86 which itself is projected from curve 88 is 8 nm at a peak concentration of 2×10^{19} atoms/cc. The doping concentration as shown by curve 86 decreases from 5×10^{19} atoms/cc at 115 nm to about 8×10^{17} atoms/cc at 109 nm and 1×10^{17} atoms/cc at 64.9 nm. The decrease in P concentration from 115 nm to 64.9 nm corresponds to a 20 nm per decade fall or decrease in P concentration.

It is noted that PH_3 has a sticking coefficient S of 1.0 while SiH_4 has a sticking coefficient S of 1×10^{-3} to 1×10^{-4}. The doping profile of P is a function of 1/GR where GR is the growth rate of the film.

Further, to eliminate background autodoping when an abrupt reduction in the P concentration is desired, a growth interrupt method is provided. The substrates or wafers are removed from the growth chamber or UHV-CVD to another vacuum chamber such as a load lock or transfer chamber or another UHV-CVD reactor or furnace where no PH_3 has been flown prior to loading. Then, SiH_4 and GeH_4 gases are flown in the growth chamber to coat the walls or heated surfaces of the growth chamber to bury or to isolate the P on the sidewalls. Then, the substrates or wafers are introduced or moved back into the main or growth chamber and the growth of Si or $Si_{1-X}Ge_X$ is continued. Alternatively, another UHV-CVD reactor or furnace coupled to the transfer chamber may be used to continue the growth of Si or SiGe with reduced or no P or As doping.

Another method for achieving abrupt P doping, is to grow a first epitaxial layer 80 in the range from 1 to 10 nm thick of $Si_{1-X}Ge_X$ on a substrate 82 as shown in Fig. 7. The higher the value of X the better for converting layer 80 to amorphous material by ion implantation by ions 83 shown in Fig. 8. X may be, for example, greater

than 0.5. First epitaxial layer 80 may be unstrained or a strained layer due to lattice mismatch with respect to substrate 82. A second epitaxial layer 84 may be grown over first epitaxial layer 80. Layer 84 may be Si or SiGe and may be unstrained or strained. Then using ion implantation shown in Fig. 6, the first epitaxial layer 80 may be selectively amorphized to form layer 80' shown in Fig. 8 by ions 83 with respect to layer 84 and substrate 82 at a dose in the range from about 10^{13} to about 10^{14} atoms/cm^2 or higher; layer 84 and any other Si or SiGe layers will not be amorphized. The Ge content of layer 84 and the other layers should be less than the content X in layer 80.

The critical dose for amorphization depends on the implanted species as well as on the host lattice. For example, boron does not amorphize Si at any dose, but amorphizes Ge at a dose higher than 1 X 10^{14} atoms/cm^2. Arsenic amorphizes Si at a dose of about 5 X 10^{14} atoms/cm^2, while arsenic amorphizes Ge at a dose of 1 X 10^{13} atoms/cm^2. Thus if an implant dose below the amorphization threshold in Si but above that in SiGe or Ge is used, then only the SiGe or Ge will be amorphized. The dossage peak should be adjusted to occur at the depth of the layer to be amorphized, layer 80.

Substrate 82 and first epitaxial layer 80 is then heated to a temperature in the range from 400°C to 500° for a period of time such as from 1 to 5 hours which results in solid phase recrystallization of the amorphized layer to form $Si_{1-X}Ge_X$ layer 80" shown in Fig. 9.

Recrystallization of amorphous layer 80' is dependent upon the material of the layer. Amorphous Ge recrystallizes at a temperature T greater than 350°C, while Si recrystallizes at a temperature T greater than 500°C. The combination of amorphization threshold dose and recrystallization temperature difference between Si and Ge is key to provide recrystallized layers.

The alloy SiGe recrystallization temperature will be somewhere in between Si and Ge, depending on the Ge content. If thicker doped layers are sought, which are above the critical thickness of Ge on Si, then SiGe with the highest possible Ge content (that will stay strained) should be used. To maximize the sharpness of the doping profile, the layers surrounding the doped layer should have the lowest possible Ge content (depending on the design).

Dopant activation occurs only in layer 80". Thus the doped layer thickness 80" is determined by the original epitaxial layer thickness 80. Diffusion of P dopants at the recrystallization temperature is negligible.

The above method applies to any species and not just to P. In fact getting sharp p-type implants is very much needed in the channel implant of 0.25μm PMOS and will be needed more when the gate length is shrunk. Boron cannot be used for such super retrograde profiles, and hence people have resorted to heavy ions such as In However, the degradation in channel mobility is higher in that case, and the incorporation of In at levels higher than 5 X 10^{17} atoms/cm^3 is almost impossible.

An n or p channel field effect transistor 91 is shown in Fig 9 utilizing layer 80" A dielectric layer 85 may be formed on the upper surface of layer 84 to form a gate dielectric such as silicon dioxide A gate 86 may be blanket deposited and patterned above dielectric 85 which may be polysilicon. Self aligned shallow souce and drain regions 87 and 88 may be formed in layer 84 by ion implantation using gate 86 as a mask. Sidewall spacers 89 and 90 may be formed on the sidewalls of gate 86. Source and drain regions 87' and 88' may be formed in layers 80 and 84 and substrate 82 using sidewall spacers 89 and 90 as a mask. Source 87 and 87' and drain 88 and 88' may be of one type material (n or p) and layer 80" may be of the opposite type material. Layer 80" functions to adjust the threshold voltage of the field effect transistor 91, prevent short channnel effects and prevent punch through between source and drain.

Referring to Fig. 10, an intermediate step in forming a field effect transistor is shown. A substrate 95 may be relaxed undoped SiGe. A phosphorous-doped Ge layer 96 is formed thereover as described with reference to Figs. 3 and 9 An undoped SiGe layer 97 is formed over layer 96. A strained undoped Si layer 98 may be formed over layer 97 Layer 98 is suitable for an electron or hole gas 99 to be present under proper voltage biasing conditions.

Referring to Fig. 11, field effect transistor 102 is shown. In Fig. 11, like reference numbers are used for functions corresponding to the apparatus Fig. 10. Source and drain regions 103 and 104 are formed spaced apart through layers 96-98 and into substrate 95. A gate dielectric 105 may be formed over layer 98 in the region between source 103 and drain 104. A gate electrode 106 of polysilicon or metal may be blanket deposited and patterned. Alternately, gate dielectric 105 may be deleted and a gate electrode of metal may form a Schottky barrier with layer 98.

Referring to Fig. 12, a cross section view of field effect transistor 110 is shown with raised source 40' and drain 40". In Fig. 12 like references are used for functions corresponding to the apparatus of Figs. 3 and 9. Substrate 82' has a layer of field oxide 112 thereover with an opening 113 formed therein. In opening 113, a gate dielectric 85 is formed on substrate 82'. A gate electrode 86 is formed such as from polysilicon and a shallow source 87 and drain 88 are formed by, for example, ion implantation self aligned with respect to gate electrode 86. Next, sidewalls 89 and 90 are formed on either side of gate electrode 86. Next, a layer 36' is selectively formed epitaxially on shallow source 87 and drain 88 on substrate 82'which is phosphorous or arsenic doped. Layer 36' is Ge or substantially Ge and corresponds to layer 36 in Fig. 3. Above layer 36', layer 40' of Si or SiGe is selectively formed epitaxially which is phosphorous or arsenic doped during fabrication. Layer 40' forms source 117 above shallow source 87 and forms drain 118 above shallow drain 88. Metal silicide contacts (not shown) may be made to source 117 and drain 118.

Claims

1. A structure having an abrupt doping profile comprising:

   a single crystal semiconductor substrate (32) having an upper surface,
   a first epitaxial layer (36) of Ge over said upper surface, said first epitaxial layer having a thickness less than the critical thickness, and having a concentration of dopant greater than 5×10^{19} atoms/cc, said dopant being selected from the group consisting of phosphorus and arsenic, and
   a second epitaxial layer (40) of a semiconductor material over said first epitaxial layer.

2. The structure of claim 1 wherein said second layer comprises a material selected from the group consisting of Si and SiGe.

3. The structure of claim 1 or 2 wherein said first layer has a thickness in the range from 0.5 to 2 nm.

4. The structure of any preceding claim wherein said second layer has a concentration change from said first layer into 40Å (4nm) of said second layer of greater than 1×10^{19} atoms/cc.

5. The structure of any preceding claim further including a third epitaxial layer of semiconductor material having a doping profile with a dopant concentration less than 5×10^{18} atoms/cc.

6. The structure of any preceding claim wherein said second epitaxial layer has a thickness of at least 300Å (30nm) and has a doping of phosporus less than 5×10^{16} atoms/cc for a predetermined thickness after its initial 300Å (30nm) thickness.

7. A method for forming an abrupt doping profile comprising the steps of:

   providing a single crystal semiconductor substrate having a major upper surface,
   forming a first epitaxial layer of Ge over said upper surface, said first epitaxial layer having a thickness less than the critical thickness,
   said step of forming the first epitaxial layer including the step of incorporating a concentration of dopant greater than 5×10^{19} atoms/cc, said dopant being selected from the group consisting of phosphorus and arsenic, and
   forming a second epitaxial layer of a semiconductor material over said first epitaxial layer

8. The method of claim 7 wherein said step of providing comprises providing a plurality of substrates, each substrate having a major upper surface, and wherein said steps of forming said first and second epitaxial layers are performed with respect to said plurality of substrates

9. The method of claim 7 or 8 wherein said step of forming said first epitaxial layer further includes the steps of placing said substrate in a CVD reactor and flowing a germanium containing gas and a dopant containing gas.

10. The method of any of claims 7-9 wherein said step of forming said first epitaxial layer further includes the step of adjusting the growth rate of said first epitaxial layer as a function of time.

11. The method of claim 10 as dependent on claim 9, wherein said step of adjusting the growth rate further includes the step of changing the flow rate of said germanium containing gas.

12. The method of any of claims 7-11, wherein said step of forming said first epitaxial layer is terminated prior to reaching the critical thickness of said first epitaxial layer.

13. The method of any of claims 7-12 wherein said step of forming said second epitaxial layer further includes the steps of placing said substrate in a CVD reactor and flowing a silicon containing gas and a dopant containing gas, said dopant being selected from the group consisting of phosphorus and arsenic.

14. The method of claim 13 wherein said step of forming said second epitaxial layer further includes the step of adjusting the flow rate of said dopant containing gas as a function of time.

15. The method of claim 13 or 14, wherein said step of forming said second epitaxial layer includes after the step of forming said first epitaxial layer, the steps of removing said substrate from said first CVD reactor to a load lock having a controlled atmosphere to prevent oxidation of the surface of said layer, and transferring said substrate to a second CVD reactor having internally exposed surfaces initially free of phosphorus.

16. The method of claim 13 or 14, wherein said step of forming said second epitaxial layer includes the steps of

   removing said substrate from said the CVD reactor to a load lock having a controlled atmosphere to prevent oxidation of the surface of said layer:
   flowing a silicon containing gas into the CVD

having heated surfaces to coat said heated surfaces with a third silicon containing layer to cover said heated surfaces that may contain phosphorus containing layers that may have formed during the formation of said first epitaxial layer;
transferring said substrate back into the CVD reactor, and
forming a fourth layer on the upper surface of said second epitaxial layer.

17. The method of claim 16 wherein said step of flowing a silicon containing gas includes the step of flowing the combination of $H_2/SiH_4/GeH_4$.

18. A method for forming abrupt doping within a semiconductor layered structure comprising the steps of:

selectively amorphizing a first layer having a high Ge content greater than 0.5, and
crystallizing said amorphized first layer by solid phase regrowth.

19. The method of claim 18 wherein said step of selectively amorphizing includes the step of ion implantation.

20. The method of claim 18 or 19 wherein said step of selectively amorphizing includes forming second and third layers above said first layer, said second and third layers having a Ge content less than 0.5.

21. A field effect transistor (91) comprising

a single crystal substrate (82) having a source region (87) and a drain region (88) with a channel therebetween and a gate electrode (86) above said channel to control charge in said channel, and
a first layer of Ge (80') less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic positioned below said channel and extending through said source and drain regions.

22. The field effect transistor of claim 21 wherein said channel is in a second epitaxial layer selected from the group consisting of Si and SiGe formed over said first layer.

23. A field effect transistor (102) comprising:

a single crystal substrate (95),
a first layer (96) of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic formed on said substrate,
a second layer (97) of undoped SiGe epitaxially formed on said first layer,
a third layer (98) of strained undoped semiconductor material selected from the group consisting of Si and SiGe, and
a source region (103) and a drain region (104) with a channel therebetween, and a gate electrode (106) above said channel to control charge in said channel.

24. A field effect transistor (110) comprising:

a single crystal substrate (82),
an oxide layer (112) formed on said substrate having an opening (113),
a gate dielectric (85) and gate electrode (86) formed in said opening over said substrate,
a source and drain region (117, 118) formed in said substrate aligned with respect to said gate electrode,
a dielectric sidewall spacer (89, 90) formed on either side of said gate electrode and above a portion of said source and drain regions,
a first layer (36') of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic selectively positioned over exposed portions of said source and drain regions,
a second layer (40') of semiconductor material selected from the group consisting of Si and SiGe doped with a dopant selected from the group consisting of phosphorus and arsenic epitaxially formed over said first layer to form raised source and drain regions.

25. The field effect transistor of any of claims 21 to 24 wherein said layer of Ge is in the range from 0.5 to 2 nm thick.

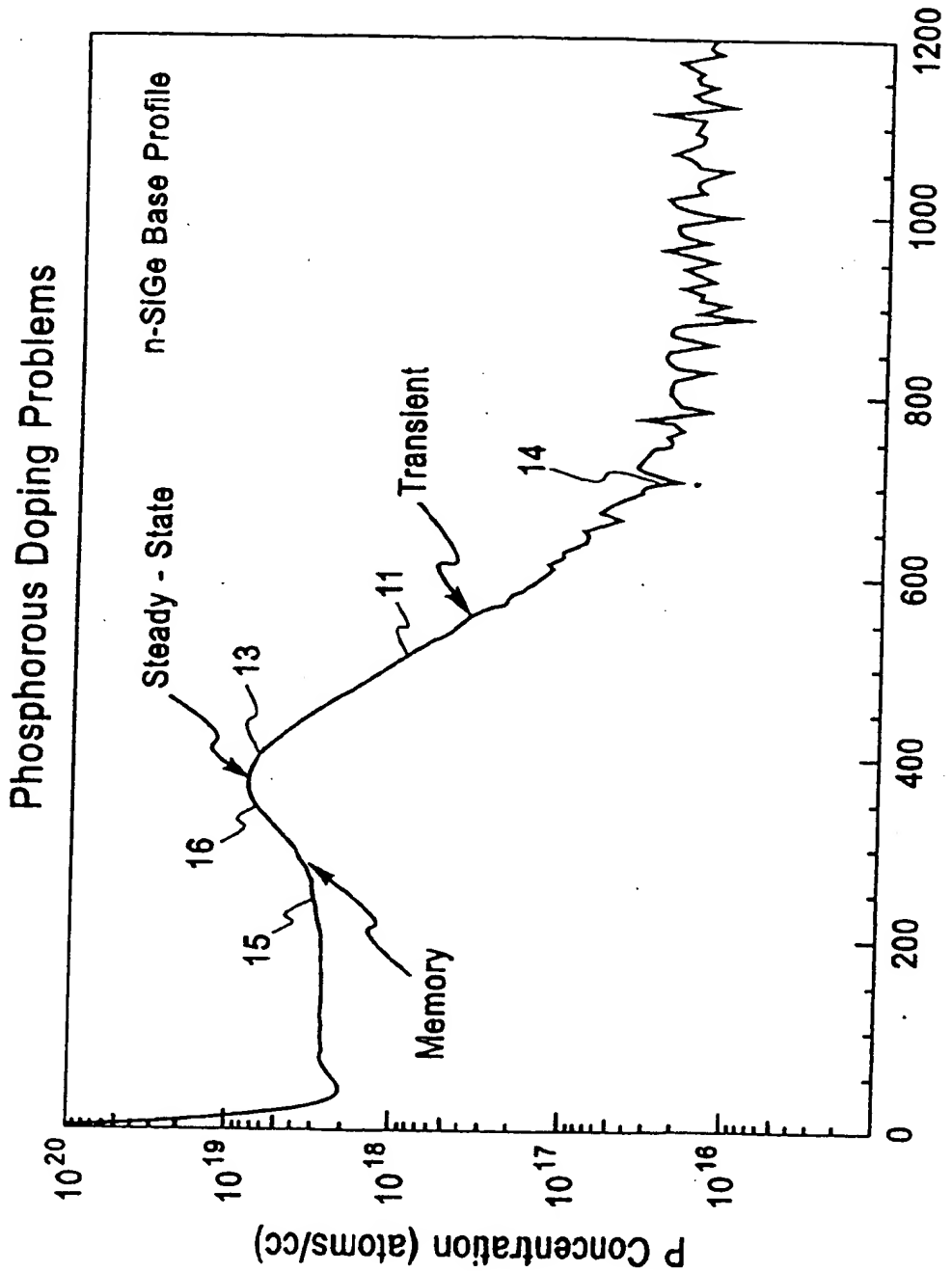

Phosphorous Doping Problems
n-SiGe Base Profile
Steady - State
Transient
Memory
11
13
14
15
16
P Concentration (atoms/cc)
Depth (Å)
10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
0
200
400
600
800
1000
1200

Fig. 1

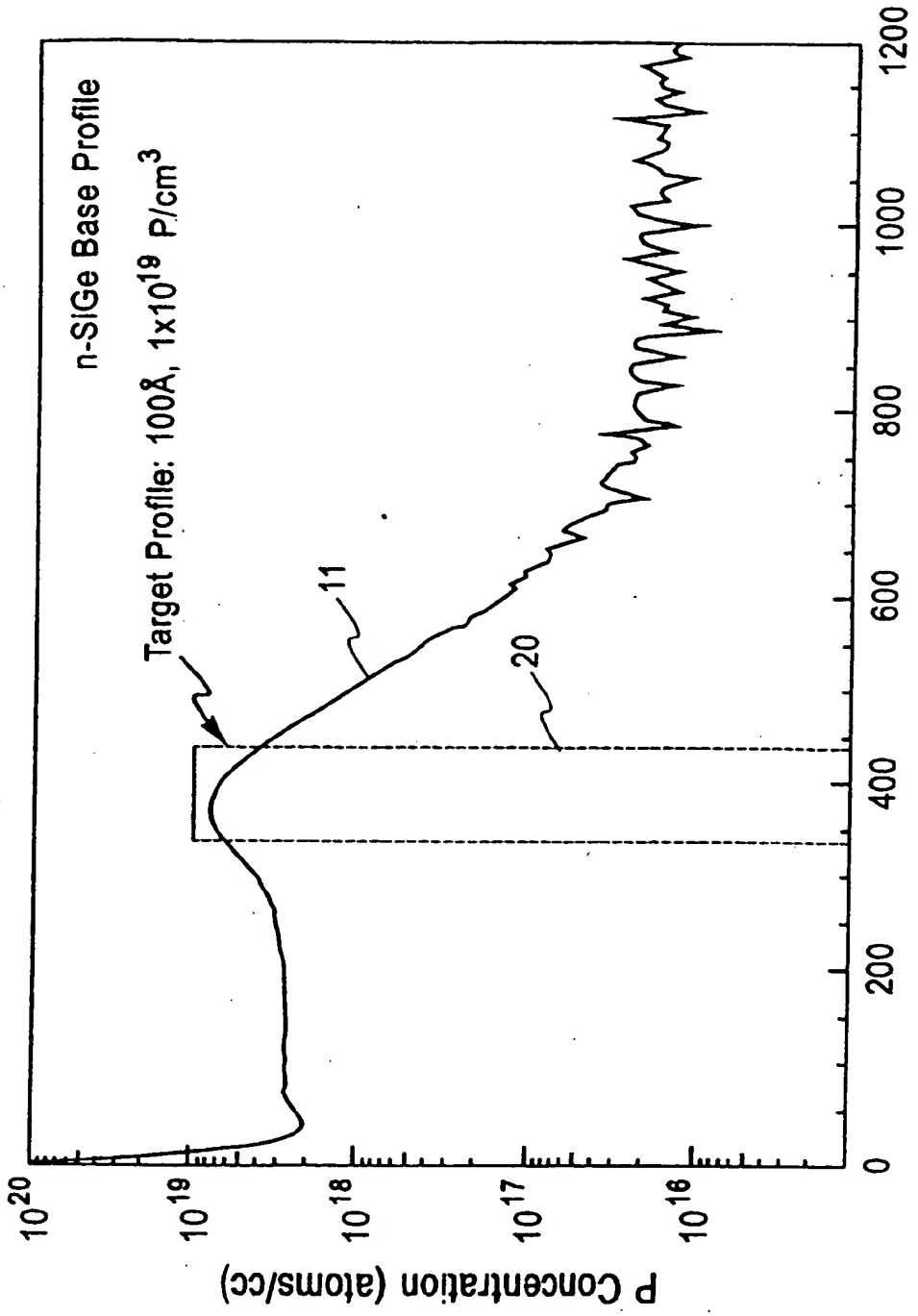

n-SiGe Base Profile
Target Profile: 100Å, 1x10^19 P/cm^3
11
20
P Concentration (atoms/cc)
10^20
10^19
10^18
10^17
10^16
0
200
400
600
800
1000
1200
Depth (Å)

Fig. 2

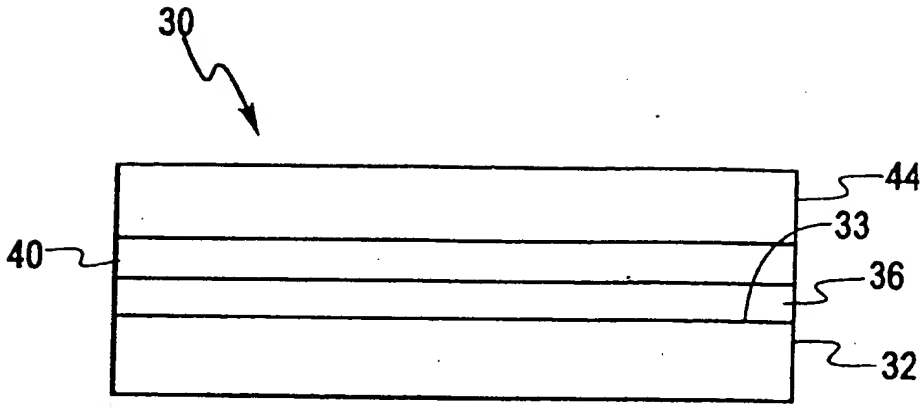


Fig. 3

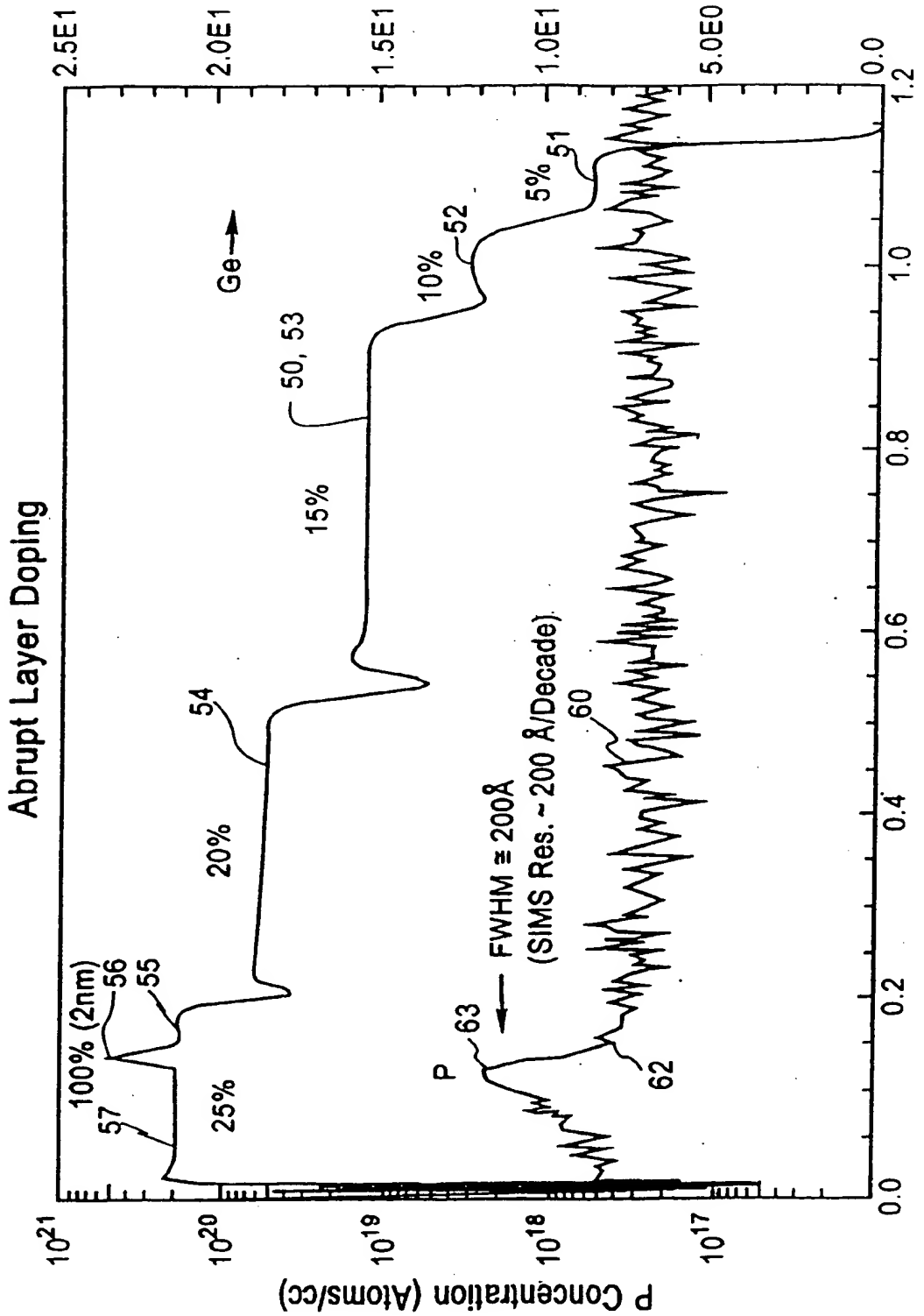

Abrupt Layer Doping
P Concentration (Atoms/cc)
Approximate Depth (μm)
Ge
100% (2nm)
25%
20%
15%
10%
5%
FWHM ≡ 200Å
(SIMS Res. ~ 200 Å/Decade)
P
50, 53
51
52
54
55
56
57
60
62
63

Fig. 4

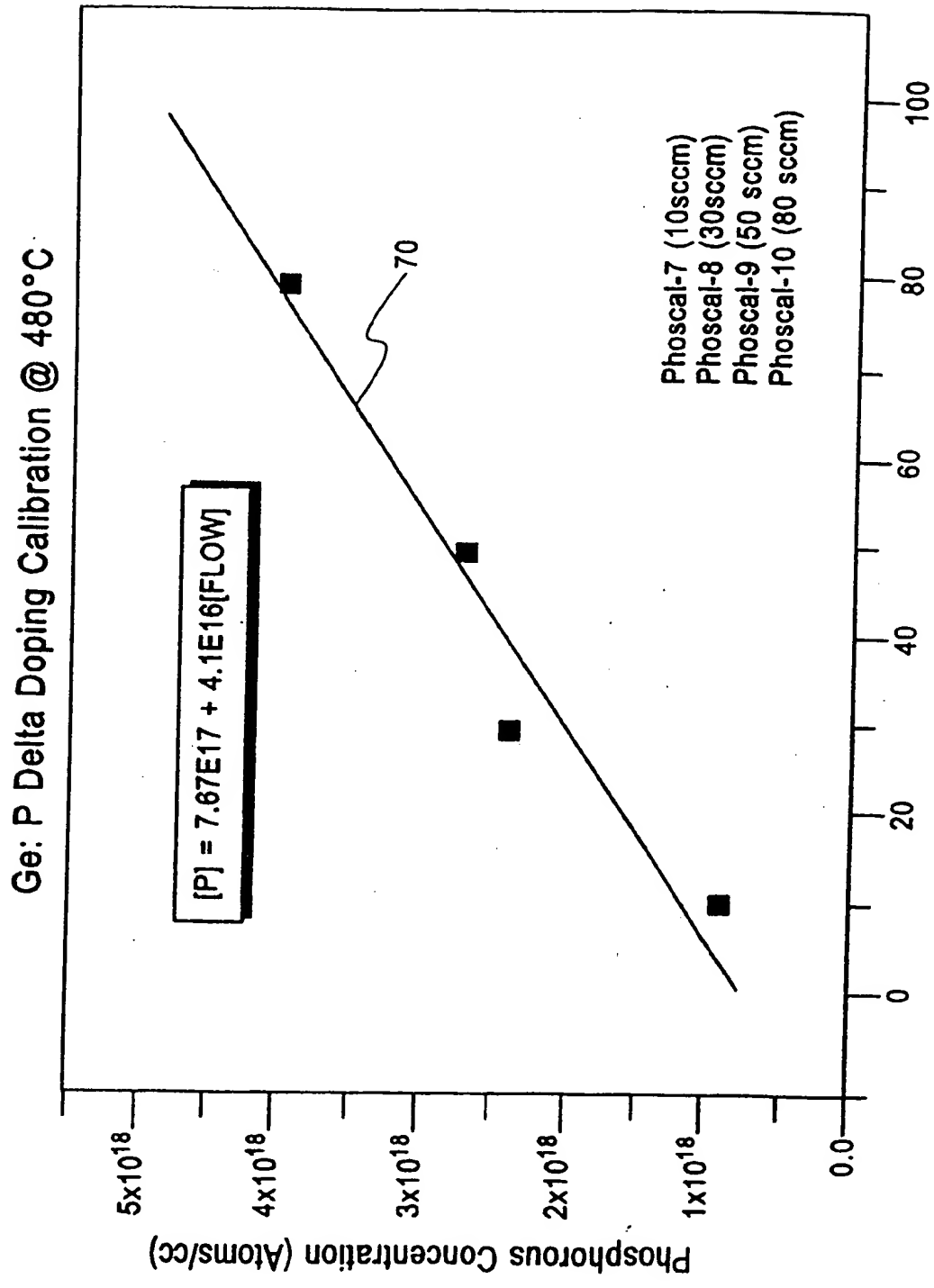

Ge: P Delta Doping Calibration @ 480°C
[P] = 7.87E17 + 4.1E16[FLOW]
70
Phoscal-7 (10sccm)
Phoscal-8 (30sccm)
Phoscal-9 (50 sccm)
Phoscal-10 (80 sccm)
Phosphorous Concentration (Atoms/cc)
5x10^18
4x10^18
3x10^18
2x10^18
1x10^18
0.0
0
20
40
60
80
100
100 PPM PH3/He Mixture Flow (sccm)

Fig. 5

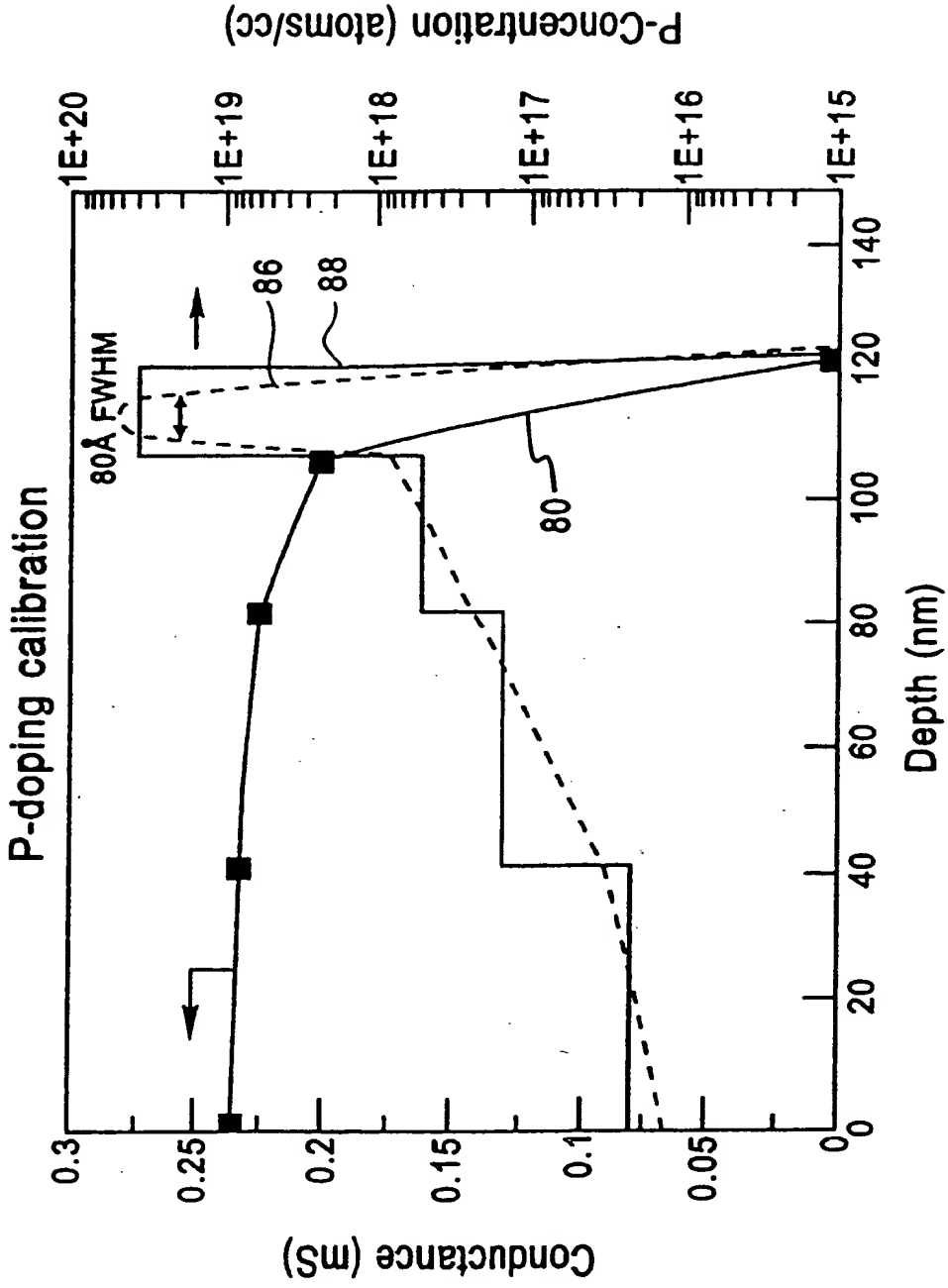

P-Concentration (atoms/cc)
1E+20
1E+19
1E+18
1E+17
1E+16
1E+15
P-doping calibration
80Å FWHM
86
88
80
Depth (nm)
0
20
40
60
80
100
120
140
Conductance (mS)
0.3
0.25
0.2
0.15
0.1
0.05
0

Fig. 6

Fig. 7

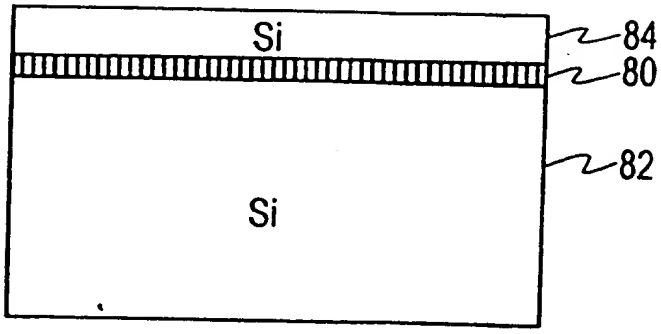


Fig. 8

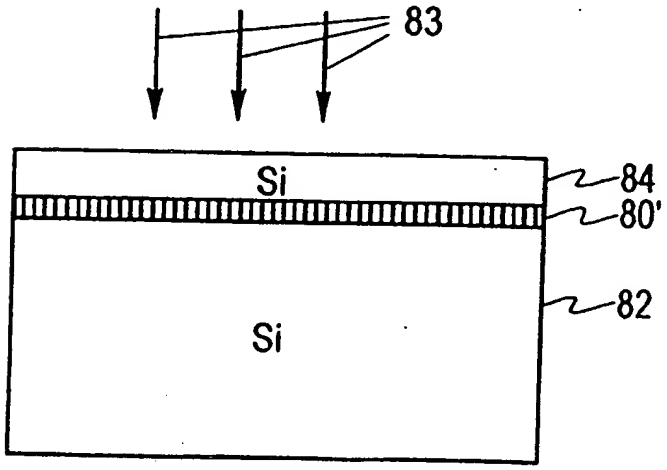
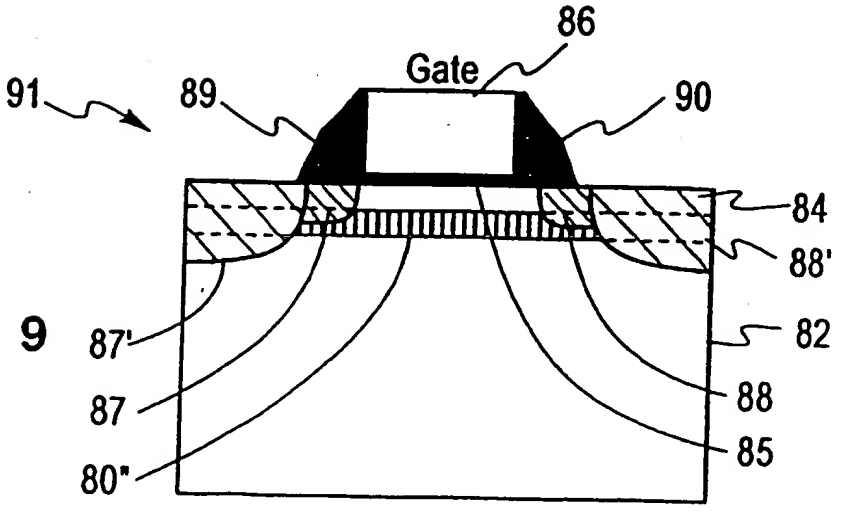


Fig. 9



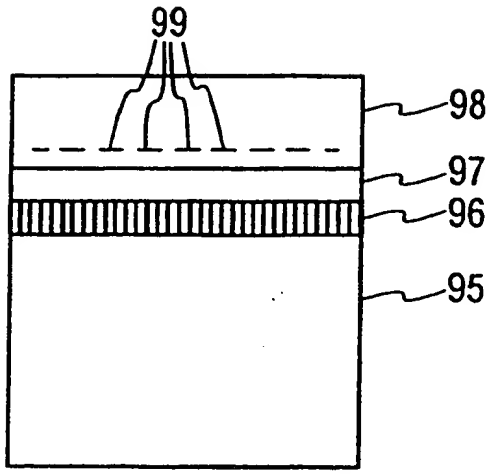

99
98
97
96
95

Fig. 10

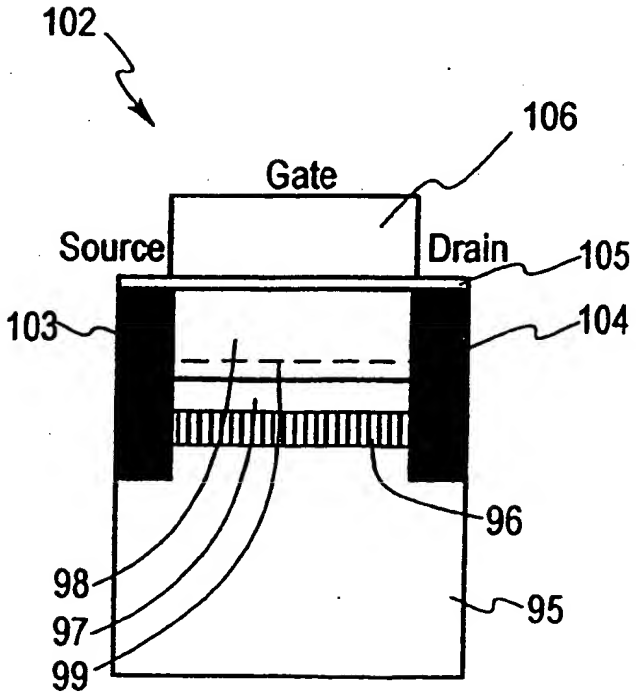

102
106
Gate
Source
Drain
105
103
104
96
98
97
99
95

Fig. 11

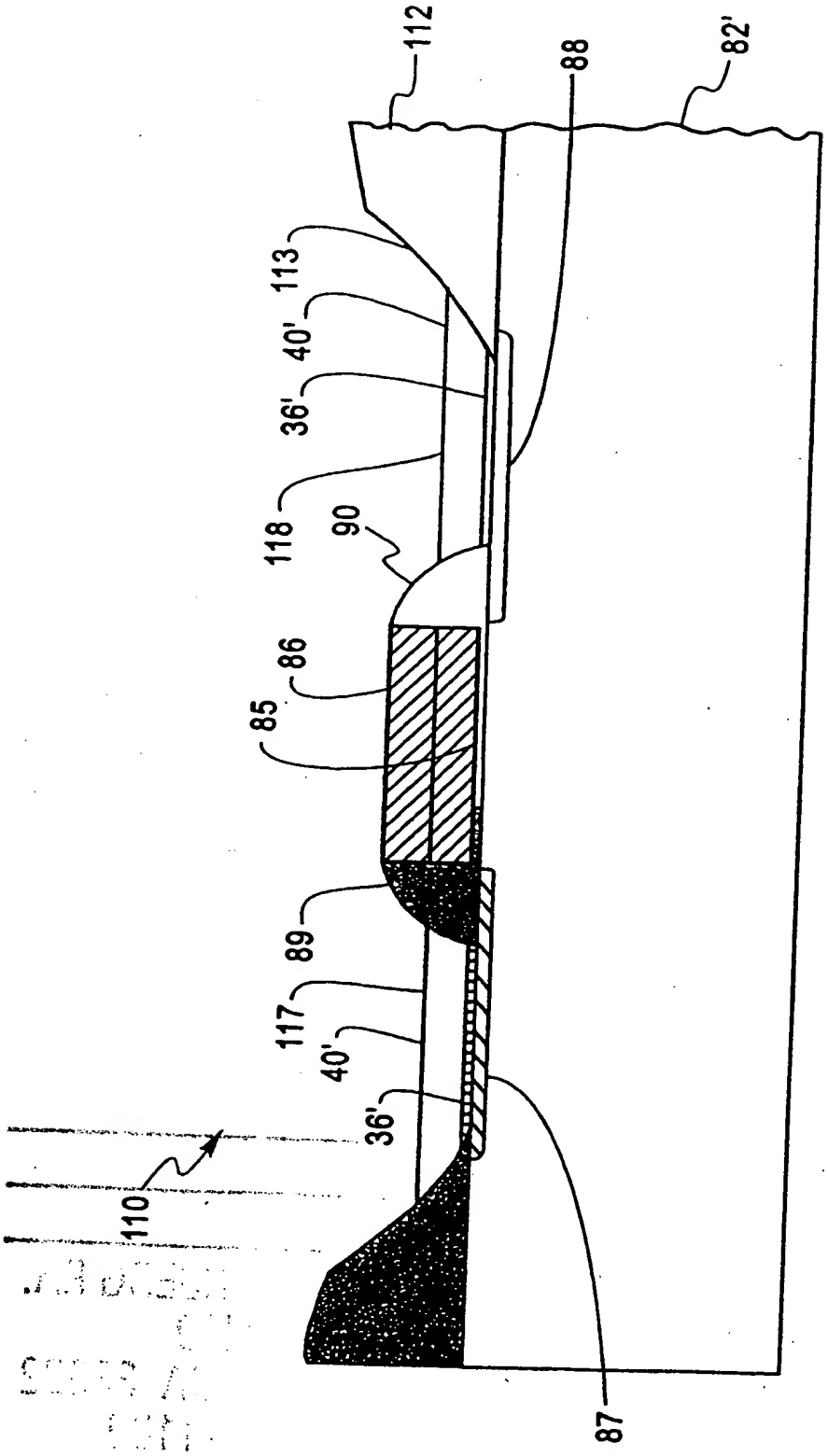


Fig. 12

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